I CLAIM:

1. A demodulator for demodulating digital data, comprising:

a receiver for receiving a digital data signal;

a determining device to determine if a fractional sample delay added to a demodulator's symbol sampling timing would improve synchronization timing;

an implementing device implementing the fractional sample delay if said determining device determines that a fractional sample delay would improve the demodulation synchronization timing; and

a demodulating device for demodulating the digital data signal.

2. A demodulator for demodulating digital data according to Claim 1, wherein said determining device comprises an algorithm that determines if a fractional sample delay would improve the demodulation synchronization timing.

3. A demodulator for demodulating digital data according to Claim 2, wherein the algorithm comprises exploiting the geometry of a correlation curve to determine if a fractional sample delay would improve the demodulation synchronization timing.

4. A demodulator for demodulating digital data according to Claim 3, wherein the algorithm further comprises comparing first and last correlation values ~~of the correlation curve that exceed a threshold value.~~

5. A demodulator for demodulating digital data according to Claim 3, wherein the algorithm further comprises counting correlation values of the correlation curve that exceed a threshold value.

6. A demodulator for demodulating digital data according to Claim 4, wherein said determining device further determines an amount of fractional sample delay necessary to improve the demodulation synchronization timing.

7. A demodulator for demodulating digital data according to Claim 5, wherein said determining device further determines an amount of fractional sample delay necessary to improve the demodulation synchronization timing.

8. A demodulator for demodulating digital data according to Claim 1, wherein the fractional sample delay is in the range of –0.5 to 0.5.

9. A demodulator for demodulating digital data according to Claim 8, wherein the fractional sample delay is selected from the group consisting of ± ¼ and ½.

10. A system for demodulating digital data according to Claim 1, wherein said implementing device comprises an interpolation filter that implements the fractional sample delay.

11. A demodulator for demodulating digital data according to Claim 10, wherein the interpolation filter comprises the steps of (i) multiplying first and second samples of each pair of input samples by respective coefficients to obtain two fractional values, and (ii) summing the fractional values.

12. A demodulator for demodulating digital data according to Claim 11, wherein said implementing device uses respective coefficients of 0.5 and 0.5 to implement a fractional sample delay of ½ sample.

13. A demodulator for demodulating digital data according to Claim 11, wherein said implementing device uses respective coefficients of 1.0 and 0.0 to implement a fractional sample delay of 0 samples.

14. A demodulator for demodulating digital data according to Claim 1, wherein said demodulator comprises the demodulator portion of a VDL Mode 2 receiver.

15. A method for demodulating digital data, comprising the steps of:

receiving a digital data signal;

determining if a fractional sample delay added to a demodulator's symbol sampling timing would improve synchronization timing;

implementing the fractional sample delay if it is determined in said determining step that a fractional sample delay would improve the demodulation synchronization timing; and

demodulating the digital data signal.

16. A method for demodulating digital data according to Claim 15, wherein said determining step comprises an algorithm that determines if a fractional sample delay would improve the demodulation synchronization timing.

17. A method for demodulating digital data according to Claim 16, wherein the algorithm comprises exploiting the geometry of a correlation curve to determine in said determining step if a fractional sample delay would improve the demodulation synchronization timing.

18. A method for demodulating digital data according to Claim 17, wherein the algorithm further comprises comparing first and last correlation values ~~of the correlation curve that exceed a threshold value.~~

19. A method for demodulating digital data according to Claim 17, wherein the algorithm further comprises counting correlation values of the correlation curve that exceed a threshold value.

20. A method for demodulating digital data according to Claim 18, wherein said determining step further comprises determining an amount of fractional sample delay necessary to improve the demodulation synchronization timing.

21. A method for demodulating digital data according to Claim 19, wherein said determining step further comprises determining an amount of fractional sample delay necessary to improve the demodulation synchronization timing.

22. A method for demodulating digital data according to Claim 15, wherein the fractional sample delay is in the range of –0.5 to 0.5.

23. A method for demodulating digital data according to Claim 22, wherein the fractional sample delay is selected from the group consisting of ± ¼ and ½.

24. A method for demodulating digital data according to Claim 15, wherein said implementing step comprises an interpolation filter that implements the fractional sample delay.

25. A method for demodulating digital data according to Claim 24, wherein the interpolation filter comprises the steps of (i) multiplying first and second samples of each pair of input samples by respective coefficients to obtain two fractional values, and (ii) summing the fractional values.

26. A method for demodulating digital data according to Claim 25, wherein a fractional sample delay of 0 samples is implemented in said implementing step by using respective coefficients of 1.0 and 0.0.

27. A method for demodulating digital data according to Claim 25, wherein a fractional sample delay of ½ sample is implemented in said implementing step by using respective coefficients of 0.5 and 0.5.

28. A method for demodulating digital data according to Claim 15, wherein a VDL Mode 2 radio receiver is provided for implementing the method.

29. A method for demodulating digital data according to Claim 15, wherein a digital circuit is provided for implementing the method.

30. A method for demodulating digital data according to Claim 15, wherein a processor is provided for implementing the method.

31. Computer executable code for implementing a method for demodulating digital data, said code for executing the steps comprising:

receiving a digital data signal;

determining if a fractional sample delay added to a demodulator's symbol sampling timing would improve synchronization timing;

implementing the fractional sample delay if it is determined in said determining step that a fractional sample delay would improve the demodulation synchronization timing; and

demodulating the digital data signal.

32. Computer executable code for implementing a method for demodulating digital data according to Claim 31, wherein said determining step comprises an algorithm that determines if a fractional sample delay would improve the demodulation synchronization timing.

33. Computer executable code for implementing a method for demodulating digital data according to Claim 32, wherein the algorithm comprises exploiting the geometry of a correlation curve to determine in said determining step if a fractional sample delay would improve the demodulation synchronization timing.

34. Computer executable code for implementing a method for demodulating digital data according to Claim 33, wherein the algorithm further comprises comparing first and last correlation values of the correlation curve that exceed a threshold value.

35. Computer executable code for implementing a method for demodulating digital data according to Claim 33, wherein the algorithm further comprises counting correlation values of the correlation curve that exceed a threshold value.

36. Computer executable code for implementing a method for demodulating digital data according to Claim 34, wherein said determining step further comprises determining an amount of fractional sample delay necessary to improve the demodulation synchronization timing.

37. Computer executable code for implementing a method for demodulating digital data according to Claim 35, wherein said determining step further comprises determining an amount of fractional sample delay necessary to improve the demodulation synchronization timing.

38. Computer executable code for implementing a method for demodulating digital data according to Claim 31, wherein said implementing step comprises an interpolation filter that implements the fractional sample delay.

39. Computer executable code for implementing a method for demodulating digital data according to Claim 38, wherein the interpolation filter comprises the steps of (i) multiplying first and second samples of each pair of input samples by respective coefficients to obtain two fractional values, and (ii) summing the fractional values.

40. Computer executable code according to Claim 30, wherein a computer readable medium is provided for storing the computer executable code.

41. A method for demodulating digital data, comprising the steps of:

receiving a digital data signal;

determining an amount of fractional sample delay to be added to a demodulator's symbol sampling timing;

implementing the fractional sample delay; and

demodulating the digital data signal.

42. A demodulator for demodulating digital data, comprising:

receiving means for receiving a digital data signal;

determining means for determining an amount of a fractional sample delay to be added to a demodulator's symbol sampling timing;

implementing means for implementing the fractional sample delay; and

demodulating means for demodulating the digital data signal.